An AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistor With Improved Breakdown Voltage for X- and Ku-Band Power Applications

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***Abstract*—This work determined that RF drain current degradation is responsible for the poor power performance of wide-recessed PHEMT. A model based on surface states was proposed to explain this phenomenon, which then led to the use of charge-screen layers and a double-recessed gate process to suppress surface effects. Combined, these two modifications increased the device's gate-drain reverse breakdown voltage without causing a degradation in the transistor's RF drain current. This allowed the simultaneous achievement of high power-added efficiency and high power density which established a new performance record for power PHEMTs at X- and Ku-bands. Delay time analyses of single- and double-recessed PHEMTs revealed that the benefit of a larger breakdown voltage in the latter device design came at the cost of a larger drain delay time. Drain delay accounted for 45% of the total delay when the 0.35 μm, double-recessed PHEMT was biased at $V_{ds} = 6$ V.**

I. Introduction

THE PERFORMANCE of active devices for high-frequency, low-noise applications advanced significantly during the past decade since the discovery of High Electron Mobility Transistors (HEMTs). Research efforts clearly established the AlGaAs/GaAs HEMT and the pseudomorphic HEMT (PHEMT) [1] as the best GaAs-based, low noise transistors for frequencies up to 60 GHz at room temperature.

For power applications, PHEMTs have found uses as millimeter-wave power transistors [2], [3] because they have higher power gain than conventional MESFETs; gain is the overriding concern at mm-wave frequencies. At microwave frequencies (X- and Ku-band in particular), PHEMTs do not compare well with MESFETs in terms of the overall power performance; that is, output power, power-added efficiency (PAE), and gain. We believe PHEMTs' inadequacy at microwave frequencies is due to a low gate-drain reverse breakdown voltage (BV_{gd}) which limits their ability to achieve high power and efficiency simultaneously. The studies cited in [2] and [3] reported BV_{gd}'s in the range of -7 to -9 V at, presumably, -1 mA/mm of leakage current. In this work, the gate-drain reverse breakdown voltage is also defined at -1 mA/mm of gate leakage current. To the best of our knowledge, a low BV_{gd} is characteristic of conventional PHEMTs.

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BV_{gd} and the pinch-off voltage determine the maximum drain voltage of a FET. For a given dc power level, it may be more advantageous to bias a power FET at high drain voltage and low drain current rather than vice versa for three reasons. One, it provides a better broadband match to 50 Ω systems. Two, a high drain voltage that translates to high RF voltage gain is preferable since the dominant circuit loss is resistive. Three, for a given output power, the overall system efficiency is improved if FETs are biased at high drain voltages due to a fixed voltage loss in the dc power supply circuit. These are some of the reasons for increasing BV_{gd} (particularly when operating FETs in Class AB or B amplifiers) and accordingly, justify the development of a PHEMT capable of sustaining a large drain bias.

In this paper we describe an effort to develop a PHEMT with a high gate-drain reverse breakdown voltage while maintaining the high gain attributes to a conventional PHEMT.

PHEMT for Power Applications

The epitaxial layer structure of a PHEMT intended for power applications can be divided into four components (listed in the reverse order of material growth): a n^+ GaAs Contact Layer, a N^+ AlGaAs Electron Supply Layer, a pseudomorphic InGaAs Channel Layer, and a bottom AlGaAs Electric Supply Layer for additional carriers. The Contact Layer prevents the underlying AlGaAs layer from oxidizing and greatly reduces the channel access resistance. The top and bottom AlGaAs Electron Supply Layers provide the carriers for current conduction, and the InGaAs layer is the nominal conduction channel. In the design of power transistors, the most crucial of these layers is the top AlGaAs Electron Supply Layer, on top of which is the Schottky gate. The doping in this layer is typically concentrated in a plane (pulse doping [4]), for power applications.

Of all the processing issues relevant to power transistors, the gate recess step (including the channel recess) is, in our opinion, the most critical. For low noise and high frequency applications, it is important to have a narrow recess, that is to say, a recess opening that is only slightly larger than the gate footprint. This has resulted in PHEMTs with high unity current cut-off frequency (Ft) and low noise [5], [6]. For power applications, a recess opening larger than the gate is necessary to obtain a large BV_{gd} [7]. On an $Al_{0.25}Ga_{0.75}As$ surface,

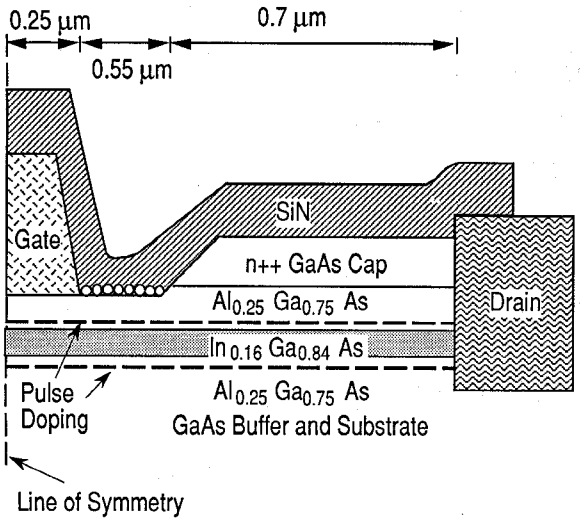


Fig. 1. A schematic of WR-PHEMT, a conventional PHEMT with a wide gate-recess. Only the gate-drain region is shown.

in addition to Tamm states, there are other surface states stemming most likely from Ga and Al oxides [8], [9] and surface impurities. Barton and Ladbrooke have suggested that these states, once occupied, increase the BV_{gd} by capturing electrons and thus decrease the electric field concentrated at the gate metal edge on the drain side [10], [11]. Indeed, our investigations showed that a BV_{gd} as high as 20 V can be achieved by simply making a wide recess in the AlGaAs electron supply layer. This simple approach has resulted in only moderate improvements in power, however.

A First Approach to Power PHEMT

Figure 1 shows a schematic of the double pulsed-doped PHEMT with wide gate-recess with its dimensions. For convenience, we denote this device that was used for this part of the work as Wide-Recess PHEMT (WR-PHEMT). The device was fabricated using a conventional planar Schottky gate process. The gate step consists of first defining gate fingers in an electron-beam resist, then recessing a gate-trench with controlled undercut to form a wide recess underneath the resist, and finally depositing gate metal. Next, a SiN "passivation" layer is deposited to protect the device from the environment. Lastly, airbridge metalization was deposited and backside processing was performed to complete the device.

The dc I–V and small signal microwave performance of WR-PHEMT are shown in Figs. 2 and 3. As is apparent from these figures, this transistor exhibited good reverse breakdown voltage and small signal performance: 450 mA/mm of maximum channel current, 21 V of gate-drain reverse-breakdown, and 13 dB of maximum stable gain (MSG) at 10 GHz. A MSG as high as 17 dB can be obtained with the appropriate bias condition. The microwave power characteristics of this device, illustrated in Fig. 4, are much poorer than the dc and small signal characteristics would suggest. At 10 GHz, the maximum PAE was only 42% with 330 mW/mm of output power. The 1 dB power compression point occurred at less than 100 mW/mm.

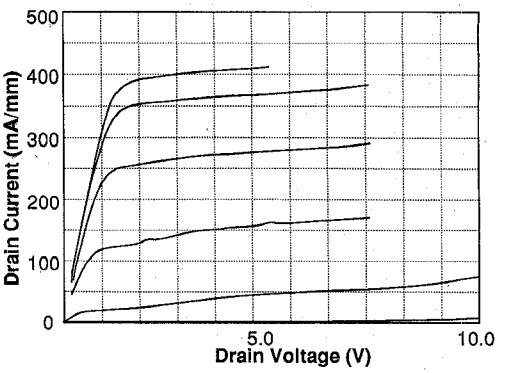


Fig. 2. The dc I–V of WR-PHEMT. The gate bias voltage starts at 0.8 V and steps toward pinch-off at −0.2V increments.

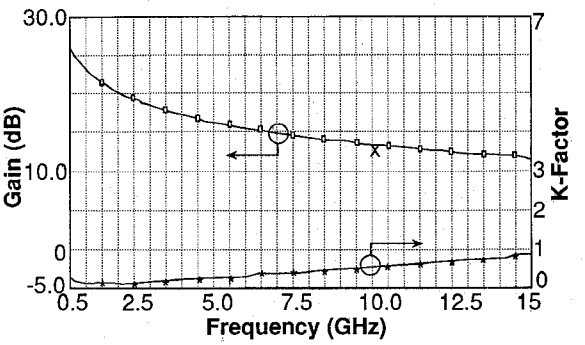


Fig. 3. Maximum stable gain and stability factor of WR-PHEMT versus frequency. The bias voltages and the resultant currents are: $V_{DS} = 6\,V, V_{GS} = 0\,V, Ids = 50$ mA/mm, $Igs = 0$ mA/mm.

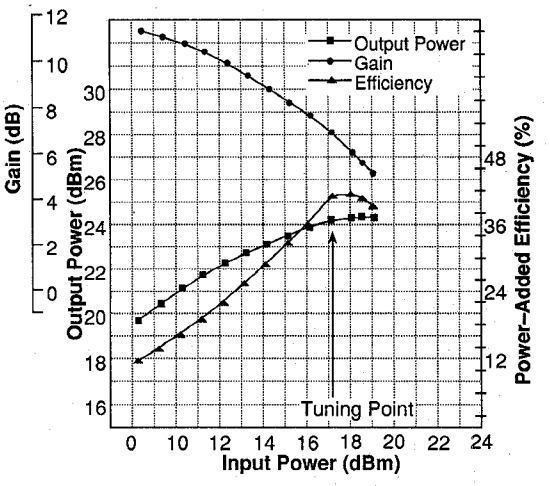


Fig. 4. Class B amplifier power performance of WR-PHEMT at 10 GHz. The bias voltages are: $V_{DS} = 6\,V, V_{GS} = -1.0\,V$. The total gate periphery is 800 μm. Notice the device has low output power despite the high maximum channel current as seen in Fig. 2.

We have attributed this transient drain current degradation to surface states. Several authors have suggested the use of non-linear transient measurements to unmask the competing effects of charge trapping and channel heating [12], [13]. One technique, called Pulsed I–V, studies a device's response to low duty-cycle, microsecond stimulations. In the conventional method, the drain and gate voltages are pulsed from zero quiescent gate-to-source voltage ($V_{GSQ} = 0\,V$) and zero

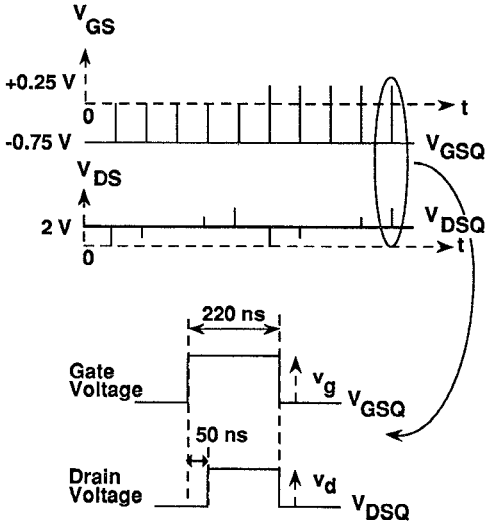


Fig. 5. A representative timing diagram of the instantaneous bias voltages. The frequency is 90 Hz.

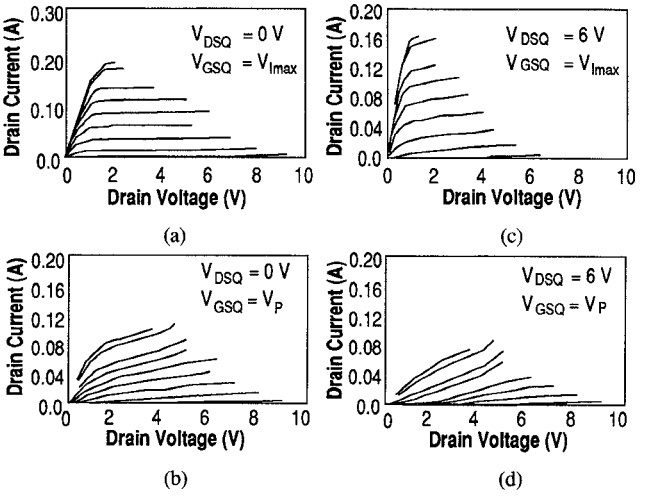


Fig. 6. Transient I–Vs of WR-PHEMT obtained by Pulsed I–V measurements. This set of figures shows the bias dependence of RF I–Vs of a device besieged by surface states. $V_{I\max}$ is defined to be at $V_{GSQ} = 1$ V and the resultant drain current is called Imax. V_p, the pinchoff voltage, is defined as the gate voltage at which the drain current is equal to 5% of Imax and $V_p = -0.6$ V for this device. The top traces are for $V_{GS} = 1.0$ V and the gate voltage step is 0.25 V. The quiescent voltages are indicated.

quiescent drain-to-source voltage ($V_{DSQ} = 0$ V) to the desired gate and drain voltages for a nanosecond duration. Transient transistor I–Vs, transfer curves, and breakdown voltages can then be measured. The instrumentation developed in our laboratory allowed the freedom to select a non-zero bias point which further aided in the diagnosis of surface problems [14].

The instantaneous gate and drain voltages, $V_{GS}(t)$ and $V_{DS}(t)$, are given by:

$$V_{GS}(t) = V_{GSQ} + V_g(t) \tag{1a}$$

$$V_{DS}(t) = V_{DSQ} + V_d(t) \tag{1b}$$

where $V_g(t)$ and $V_d(t)$ are the respective ac voltages. A sample timing diagram of applied voltages is shown in Fig. 5 for $V_{GSQ} = -0.75$ V and $V_{DSQ} = 2$ V. The diagram illustrates the gate and drain voltage pulse trains that trace out the two I–V curves corresponding to $V_{GS}(t) = 0$ and 0.25 V with $V_{DS}(t)$ varying from 0 to 4 V in 1 V steps.

The transient I–V's of WR-PHEMT are shown in Fig. 6. This device showed a strong transient I–V dependence on the quiescent gate or drain biases. Drain current and transconductance both decrease for either more negative gate voltages or larger drain voltages. However, the pinchoff voltage remained the same. The advantage of being able to pulse from any quiescent bias is suggested in this figure: setting the quiescent bias in effect selects particular traps in the gate-drain region for the pulsed I–V analysis.

A Parasitic Gate

Degradation in transient drain current had been observed in MESFETs [15]. However, the problem is rarely as severe as we observed in the WR-PHEMT. The shallowness of the active channel and the nature of AlGaAs surfaces are probably the main reasons that PHEMTs are much more sensitive to the surface than conventional MESFETs. We believe that the cause of severe RF current degradation in WR-PHEMTs is due to "parasitic gating" from surface charges, which is the same agent that alleviates the high electric field at the gate metal edge on the drain side. We consider two plausible mechanisms which could give rise to a "parasitic gate."

In the first model, we assumed the surface was depleted such that an inversion layer was formed. Fermi level pinning at the surface $Al_{0.25}Ga_{0.75}As$ was taken to be 0.58 eV above the valence band edge. This is derived from a linear extrapolation of the surface pinning energies of GaAs and AlAs [16]. A parasitic gate was then formed by a surface inversion layer resulting from the exposed $Al_{0.25}Ga_{0.75}As$ in the gate-drain region. Such a surface inversion layer has a hole density calculated to be ~ 100 per cm^2, corresponding to a sheet resistance on the order of $10^{14}\,\Omega$/sq. A typical fringing capacitance of 0.15 pF/mm between the gate and drain electrodes gives rise to a RC time constant of several milliseconds. This model explained the time delay in drain current but cannot account for the variations in pulsed I–V characteristics of different quiescent biases illustrated in Fig. 6. One might construe that this model is sufficient in light of only gate-lag (to be described later) data.

The mechanism for transferring charges onto the surface between gate and drain electrodes was included in the second model. In the presence of high electric fields in the gate drain region, electrons could spatially tunnel from metal gates to nearby surface states in the semiconductor as suggested by several researchers, see for example [10]. As the drain-gate voltage increases, those surface states further away from the gate could also be ionized as electrons transferred from the gate electrode hopped across a landscape of densely packed states on the $Al_{0.25}Ga_{0.75}As$ surface. These trapped electrons create a space charge region commensurate with their number. If we assume the re-emission rate of these trapped charges is on the order of microseconds, then the depletion region is essentially static relative to input RF stimuli. In this manner, a static parasitic gate is formed. If the input stimulation is faster than the trap response time and the region immediately to the

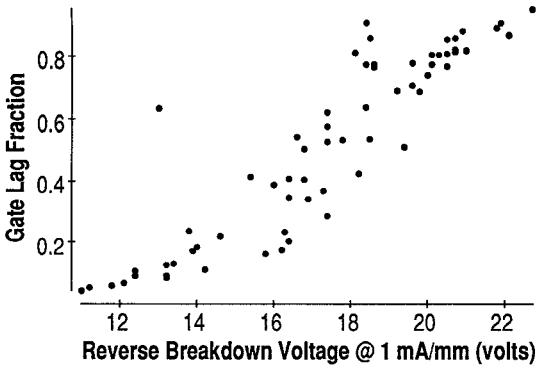


Fig. 7. Measured gate-lag fraction versus BV_{gd} of WR-PHEMT. In general, the slope and intercept of this curve depend on the epitaxial design and etch profile. It clear from this graph that breakdown voltage alone does not characterize a good power FET.

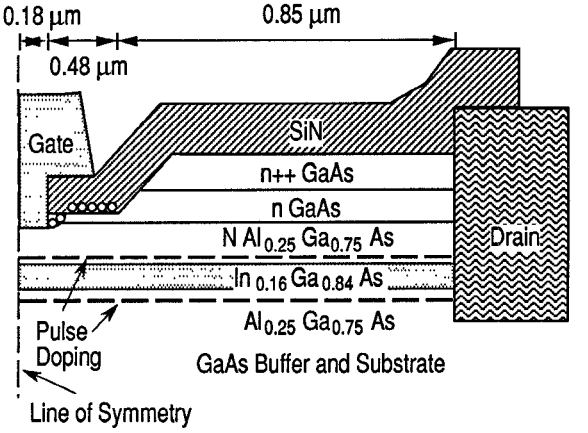


Fig. 8. A schematic of HB-PHEMT. The epitaxial material was prepared by MBE. $V_p = -1.2$ V.

drain side of the gate is populated with transferred electrons which partially deplete the channel, then only a small amount of RF current will flow in the channel due a constriction in the region between the gate and drain electrodes. Since the "parasitic gate" is controlled by the dc bias, transient I–V's show a strong bias dependence consistent with the behavior observed in Fig. 6.

The emission times of these trapped charges can be deduced from gate-lag measurements of drain current response [17]. In a gate lag measurement, a drain voltage is applied through a resistor and the gate, biased with a quiescent pinch-off voltage, is pulsed on. If the pulse width is greater than trap emission time, then the rise time of the drain current will correspond to the emission time of the surface states. A gate lag fraction of drain current can then be defined as the portion of the drain current that does not instantaneously respond to the gate action. Since BV_{gd} and gate lag are both caused by charge transfer between the gate metal and surface states, their relationship provides a telling description of the surface state effect. Fig. 7 shows the gate lag versus BV_{gd} of WR-PHEMT and thereby revealing, in another perspective, the drawback of wide recess. The figure shows that simply increasing BV_{gd} by widening the gate recess will result in a large fraction of gate-lag drain current, particularly at the higher voltages, which is too slow to respond to the RF drive.

We also studied the temperature dependence of the trap emission time. Trap emission times on the order of milliseconds were determined. Measurements of decay time constant versus temperature revealed a trap activation energy of 0.4 eV.

The collapse of pulsed I–Vs has been observed in all the pulse doped PHEMTs that we studied with wide gate recesses. It is clear that for PHEMTs to be a candidate for power applications, the effect of parasitic gating by excess surface charges must either be eliminated or screened from the active channel. The elimination of surface states is not only unattainable but also may be undesirable due to the benefit of trapped excess charges in mitigating the electric fields at the gate metal edges.

A PHEMT with Reduced Surface Effect

Screening the effect of the surface on the active region, can be accomplished by modifying the WR-PHEMT in two ways: using a double-recessed gate process, and adding charge screen layers. These modifications are shown in Fig. 8 along with dimensions. The double recess reduces the surface electric field in the immediate vicinity of the gate in the drain side [18]. In the double recess, the first, wider recess stops in a lightly doped GaAs layer, leaving a thin layer (~50 Å) of that material beneath the surface. The second, narrower recess is etched into the n-AlGaAs for the desired channel current. The gate footprint is defined by the second etch. The "charge screen" layers are made of a thin layer of doped GaAs placed just beneath the exposed surface in the channel recess and a lightly doped AlGaAs layer with a Si doping plane near the heterointerface in place of the top pulse-doped electron supply layer. If the detail charge balance is correct, the surface depletion, already reduced by the double recess, can be contained within this thin, lightly-doped layer and thereby screen the channel from surface charges. In effect the doped layers, intervening between the surface and the channel, reduce the channel charge modulation efficiency of the "parasitic gate." This device will be referred to as the High Breakdown PHEMT (HB-PHEMT). The fabrication process is identical to the WR-PHEMT described earlier with the exception of the channel recess and the dielectric-assisted T-gate process [19]. Although a 0.35-μm T-gate version is described here for the convenience of later discussions on single versus double recess, we determined in separate studies that the T-gate (either structural, i.e., dielectric-assisted versus conventional tri-layer T-gate, or process) is not a factor in the issue of parasitic gating.

The bias dependence of RF I–Vs was largely eliminated as shown in Fig. 10(a) and (b). (This is especially apparent when contrasted with the device shown in Fig. 6(a) and (d).) The BV_{gd} that corresponds to a drain-current gate lag fraction of ~0.1 has been increased from ~11 to ~15 V.

HB-PHEMT Analysis and Discussion

DC and Small Signal The HB-PHEMT described in the previous section was characterized in terms of dc, microwave small signal S-parameters, microwave power and low-noise performance.

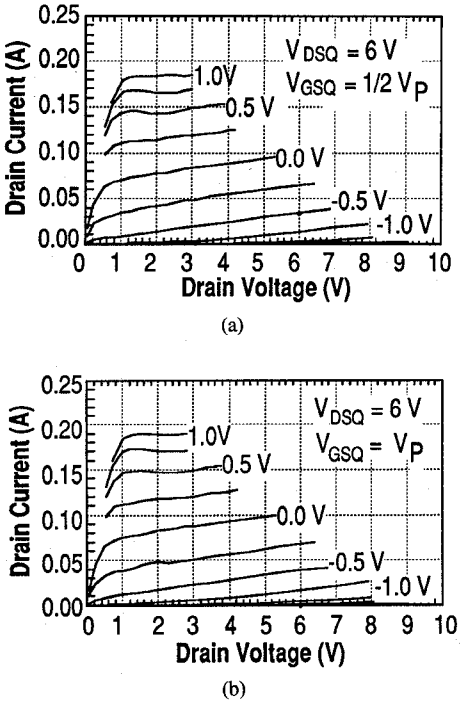


Fig. 9. Pulsed I–Vs for HB-PHEMT. The pulsed I–Vs clearly show little bias dependence.

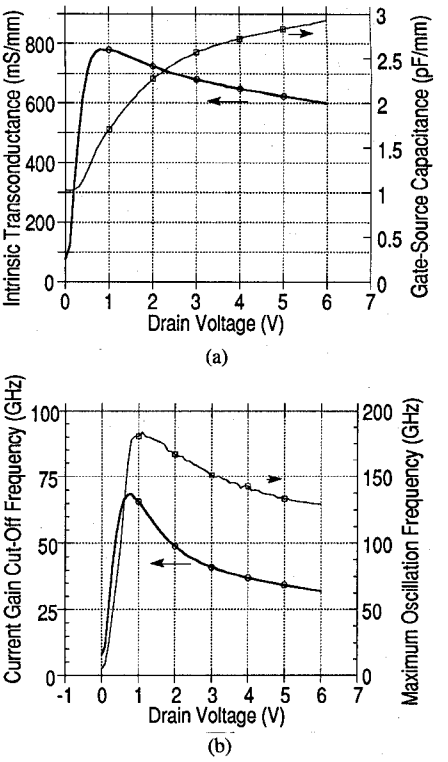


Fig. 10. Drain voltage dependence of transconductance, gate-source capacitance, current gain cut-off frequency and maximum oscillation frequency of HB-PHEMT. The gate was biased at 0.2 V for the drain scan.

All dc measurements were performed with microwave coplanar probes and bias terminations to suppress potential oscillations. The peak extrinsic transconductance was 540 mS/mm at $V_{GS} = 0.4$ V and $V_{DS} = 1.0$ V. The source and drain resistances, as determined by Fukui's end-resistance method [20], were 0.47 and 0.54 Ω-mm, respectively.

The microwave small signal equivalent circuit elements of this device were obtained using the bias scan method of Hughes and Tasker [21]. The pad capacitances were determined from a device that was lacking an active region, and the series terminal resistances and inductances were obtained from an active device biased under forward gate conduction with equal source and drain currents. The values of these parasitic elements were not affected by the gate bias in the range of interest.

HB-PHEMTs exhibited a peak maximum available power gain cut-off frequency ($F_{\max}$) of 180 GHz and an intrinsic peak unity current gain cut-off frequency (F_t) of 68 GHz (see Fig. 10(a)), all at drain voltages (<2 V) which are not particularly meaningful for power applications. A rapid decrease in $F_{\max}$ with increasing drain voltage was observed which apparently stemmed from a decrease in F_t with increasing drain bias. The decrease in F_t was attributed to a rapid increase in gate-source capacitance and a rapid decrease in transconductance as seen in Fig. 10(a). The strong drain voltage dependence of C_{gs} is atypical and cannot be explained by fringing field alone.

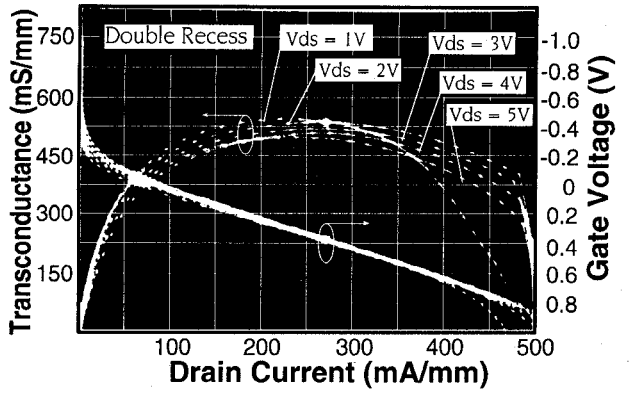
Time Delay Analysis of Single-Versus Double-Recessed PHEMT

To better understand the F_t degradation with increasing drain bias, a delay time analysis (first demonstrated by Moll *et al.* [22] for PHEMTs) was performed on the HB-PHEMT and on a single gate-recess PHEMT of the same epitaxial structure. These devices were fabricated in the same manner (identical process, including T-gates, and dimensions) as the HB-PHEMT described earlier. These two types of devices were fabricated side by side on the same wafer. The only process difference between them was the channel recess which was skipped for the single-recessed devices. A matched pair of single recess (SR) and double recess (DR) devices were chosen for study based on their similar dc characteristics. Fig. 11 shows the transfer characteristics of these two PHEMTs. Output conductance and breakdown voltage were the only significant differences observed of the dc parameters.

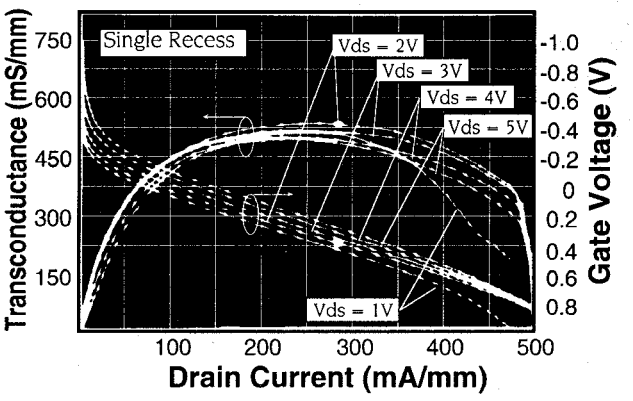
F_t, gate-source capacitance, and delay components are related by:

$$\frac{1}{F_t} = \frac{2\pi(C_{gs} + C_{gd})}{g_m} = 2\pi(t_{\rm rc} + t_d + t_i) \tag{2}$$

where $t_{\rm rc}$ is the channel charging time, t_i is the intrinsic delay time and t_d the drain delay time. These delay components can be separately determined by measuring the dependence of the total delay time $(1/2\pi F_t)$ as functions of inverse drain current and of drain voltage. The validity of this technique requires the sum of $t_{\rm rc}$ and t_i to be constant with respect to drain voltage, and of t_d and t_i to be constant with respect to inverse drain current, at a constant drain voltage. This requirement is satisfied when a linear dependence of the total delay time on intrinsic drain voltage and of total delay time on inverse drain current is observed. The extrapolations of linear regions of the data to zero drain voltage or to infinite drain current give the



(a)

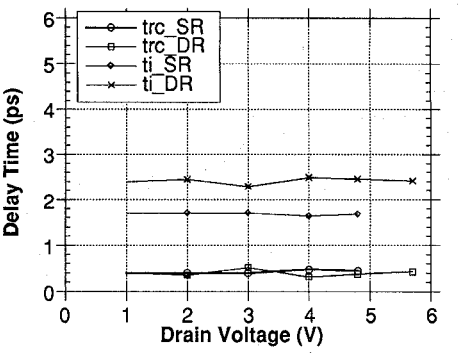


(b)

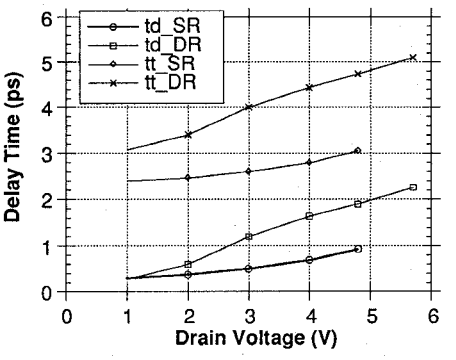
Fig. 11. DC transfer characteristics of the pair of transistors used for the drain delay analysis. BV_{gd} is -14 V for the DR device (Fig. a) and -7 V for the SR device. Source resistance is 0.44 Ω-mm for the SR device and 0.47 Ω-mm for the DR device which is larger due to the channel recess.

remaining delays $t_{rc}+t_i$ or t_d+t_i, respectively. The resultant delay times as a function of drain voltage are plotted in Fig. 12.

Fig. 12(a) shows that t_{rc} and t_i are indeed independent of drain bias. The t_{rc}'s were nearly identical to these two devices of the same epi-layer origin, which suggested the assumption was valid that this component of the delay time was due to the RC charging time of the channel. The intrinsic delay time of the SR device appeared to be shorter for unknown reasons. It is unlikely that the differences could be entirely due to minute variations in the gate length caused by channel recess. Indeed, the zero drain-bias capacitance of the SR device is no less than the DR device at all gate voltages. Regardless, the sum of t_{rc} and t_i was constant which validated the procedure for determining the drain delay. An increase in drain delay is the sole reason that the total delay time increased with drain voltage in both types of device, as is clearly evident in Fig. 12(b). The double recess improved the breakdown voltage and reduced feedback capacitance, but apparently it did so at the cost of a longer drain delay as indicated by the comparison with the SR device. At $Vds = 4.8$ V, drain delay accounted for approximately 31% of the total delay in the SR-PHEMT and 40% in the DR-PHEMT. At $Vds = 6.0$ V this number increased to 45% in the DR device. Accordingly, drain delay appears to be a limitation of using PHEMTs for large drain voltage, high frequency power operations—despite PHEMT's excellent high frequency characteristics at low drain voltages.



(a)



(b)

Fig. 12. Drain delay versus drain voltage of SR and DR PHEMT's. The drain delay increases rapidly with increasing drain voltage. At $V_{DS} = 6$ V, drain delay accounts for 45% of the total delay time (t_T).

Power and Noise Characterizations

Devices were mounted in low loss (<0.8 dB) coaxial fixtures for X- and Ku-band power and noise measurements. The amplifier tuning was performed with metal discs, and spectrum analyzers were used to monitor the output signal. The power performance of HB-PHEMT was previously reported [23]. Some of the highlights are a 0.4 mm periphery device with a PAE of 65%, a power gain of 11.8 dB and an output power of 312 mW (780 mW/mm of gate width) at 10 GHz. At the same frequency, a 1.2-mm periphery device exhibited an output power at 1.12 W with 56% PAE and 8 dB power gain. At 18 GHz, the 0.4-mm device achieved 51% PAE, 7.6 dB gain and 300 mW of output power. These results established a new power performance record for PHEMTs at X- and Ku-bands.

HB-PHEMTs were also characterized for noise, and minimum noise figures of 0.9 dB with 11.3 dB associated gain at 10 GHz and 1.5 dB with 8.0 dB gain at 18 GHz were obtained. Since the device has excellent transport properties at low drain voltages and low source resistance, its low noise and high gain figures were expected.

II. Conclusion

Pseudomorphic HEMTs for power and low noise applications at X- and Ku-band have been investigated. It was found that improving BV_{gd} by simply widening gate recesses leads to a collapse of pulsed I–V characteristics at large drain-gate voltages. This phenomenon has been attributed to surface states between the gate and drain. A field reduction and charge

screen technique was utilized to isolate the channel electrons from the surface charge while maintaining the breakdown advantage of a wide-gate recess. This led to the demonstration of high breakdown PHEMTs with record high power-added efficiency, high power and good noise characteristics at X- and Ku-bands. A study of delay times of single- and double-recessed devices showed that a drawback of the double-recessed PHEMT is the increase in drain delay time which limits their operating frequencies.

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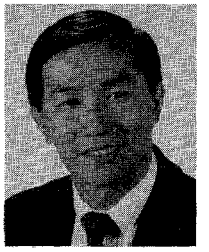
REFERENCES

[1] G. Duh, *et al.*, "Ultra low noise characteristics of millimeter-wave HEMT," *IEEE Elec. Dev. Lett.*, vol. 9, no. 10, pp. 521–523, 1988.
[2] P. M. Smith, *et al.*, "InGaAs pseudomorphic HEMTs for millimeter wave power applications," *1988 IEEE MTT-S Dig.*, pp. 927–930.
[3] P. M. Smith, et al., "A 0.15 μm gate-length pseudomorphic HEMT," *1989 IEEE MTT-S dig.*, pp. 983–986.
[4] M. Hueschen *et al.*, "Pulse doped MODFETs," *1984 IEDM Tech. Dig.*, San Francisco, CA, paper 13.3, Dec. 1984, pp. 348–351.
[5] J. C. Huang, *et al.*, "A high-gain, low noise, 1/2-μm pulse-doped pseudomorphic HEMT," *IEEE Elect. Dev. Lett.*, vol. 10, no. 11, Nov. 1989.
[6] L. Lester, *et al.*, "High efficiency 0.25-μm gate-length pseudomorphic power heterostructure FET's at mm-wave frequencies," *47th DRC Tech. Dig.*, June 1989, IVB-4.
[7] T. Furutsuka, T. Tsuji, and F. Hasegawa, "Improvement of the drain breakdown voltage of GaAs power MESFET's by a simple recess structure," *IEEE Trans. Electron Devices*, vol. ED-25, no. 6, pp. 563–567, 1978.
[8] W. F. Croyden and E. H. C. Parker, *Electrocomponent Science Monographs*. London: Gordon and Breach Science Publishers, 1981.
[9] S. G. Louie, J. R. Chelikowsky and M. L. Cohen, *J. Vac. Sci. Technol.*, vol. 13, pp. 790–797, 1976.
[10] T. M. Barton and P. H. Ladbrooke, "The role of the device surface in the high voltage behavior of the GaAs MESFET," *Solid State Electronics* vol. 29, no. 8, pp. 807–813, 1986.
[11] T. Furutsuka *et al.*, "Improvement of the drain breakdown voltage of GaAs power MESFET's by a simple recess structure," *IEEE Trans. Electron Devices*, vol. ED-25, no. 6, pp. 563–567, 1978.
[12] M. A. Smith, *et al.*, "RF nonlinear device characterization yields improved modeling accuracy," *MTT-S Dig.*, 1986, pp. 381–384.
[13] M. Paggi, *et al.*, "Nonlinear GaAs MESFET modeling using pulsed gate measurements," *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 12, pp. 1593–1597, 1988.
[14] A. Platzker, *et al.*, "Characterization of GaAs devices by a versatile Pulsed I–V measurement system," *1990 IEEE MTT Dig.*.
[15] L. D. Hou *et al.*, in *1991 GaAs Manufacturing Technology Conf. Dig.* pp. 81–84.
[16] G. Platero *et al.*, "Anion-induced surface states for the ideal (100) faces of GaAs, AlAs and GaSb," *Surface Science*, vol. 172, pp. 47–56, 1986.
[17] R. Yeats, *et al.*, "Gate slow transients in GaAs MESFETs—causes, cures and impact on circuits," *IEEE IEDM 1988 Dig.*, pp. 842–845.
[18] H. Mizuta, *et al.*, "Surface potential effect on gate-drain avalanche breakdown in GaAs MESFET's," *IEEE Trans. Electron. Dev.*, vol. ED-34, no. 10, pp. 2027, Oct. 1987.
[19] D. K. Atwood, "Vacuum passivated T-gates: A new method for fabricating submicron gates," *SPIE Proc.*, vol. 1263, pp. 209–216.
[20] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *The Bell Syst. Tech. J.*, vol. 58, no. 3, pp. 771–797, Mar. 1979.
[21] B. Hughes *et al.*, "Bias dependence of the MODFET intrinsic values at microwave frequencies," *IEEE Trans. Elect. Dev.*, vol. 36, no. 10, pp. 2267–2273, Oct. 1989.
[22] N. Moll *et al.*, "Pulsed doped AlGaAs/InGaAs pseudomorphic MODFETs," *IEEE Trans. Electron Devices* vol. 35, pp. 878–886, July 1988.
[23] J. C. Huang, *et al.*, "An AlGaAs/InGaAs pseudomorphic high electron mobility transistor (PHEMT) for X- and Ku-band power applications," *1991 IEEE MTT-S Dig.*, pp. 713–716.



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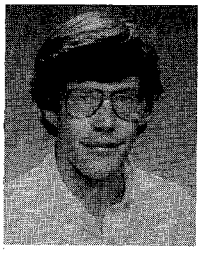

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